SSTUB32864

1.8 V configurable registered buffer for DDR2-800 RDIMM applications

Rev. 02 — 26 March 2007 Product data sheet

1. General description

The SSTUB32864 is a 25-bit 1 : 1 or 14-bit 1 : 2 configurable registered buffer designed for 1.7 V to 2.0 V V_{DD} operation.

All clock and data inputs are compatible with the JEDEC standard for SSTL_18. The control inputs are LVCMOS. All outputs are 1.8 V CMOS drivers that have been optimized to drive the DDR2 DIMM load.

The SSTUB32864 operates from a differential clock (CK and $\overline{CK}$). Data are registered at the crossing of CK going HIGH, and $\overline{CK}$ going LOW.

The C0 input controls the pinout configuration of the 1 : 2 pinout from A configuration (when LOW) to B configuration (when HIGH). The C1 input controls the pinout configuration from 25-bit 1 : 1 (when LOW) to 14-bit 1 : 2 (when HIGH).

The device supports low-power standby operation. When the reset input ($\overline{RESET}$) is LOW, the differential input receivers are disabled, and un-driven (floating) data, clock and reference voltage (VREF) inputs are allowed. In addition, when $\overline{RESET}$ is LOW all registers are reset, and all outputs are forced LOW. The LVCMOS $\overline{RESET}$ and Cn inputs must always be held at a valid logic HIGH or LOW level.

To ensure defined outputs from the register before a stable clock has been supplied, $\overline{RESET}$ must be held in the LOW state during power-up.

In the DDR2 RDIMM application, $\overline{RESET}$ is specified to be completely asynchronous with respect to CK and $\overline{CK}$. Therefore, no timing relationship can be guaranteed between the two. When entering reset, the register will be cleared and the data outputs will be driven LOW quickly, relative to the time to disable the differential input receivers. However, when coming out of reset, the register will become active quickly, relative to the time to enable the differential input receivers. As long as the data inputs are LOW, and the clock is stable during the time from the LOW-to-HIGH transition of $\overline{RESET}$ until the input receivers are fully enabled, the design of the SSTUB32864 must ensure that the outputs will remain LOW, thus ensuring no glitches on the output.

The device monitors both $D\overline{CS}$ and $\overline{CSR}$ inputs and will gate the Qn outputs from changing states when both $D\overline{CS}$ and $\overline{CSR}$ inputs are HIGH. If either $D\overline{CS}$ or $\overline{CSR}$ input is LOW, the Qn outputs will function normally. The $\overline{RESET}$ input has priority over the $D\overline{CS}$ and $\overline{CSR}$ control and will force the outputs LOW. If the $D\overline{CS}$-control functionality is not desired, then the $\overline{CSR}$ input can be hardwired to ground, in which case the set-up time requirement for $D\overline{CS}$ would be the same as for the other Dn data inputs.

The SSTUB32864 is available in a 96-ball, low profile fine-pitch ball grid array (LFBGA96) package.

2. Features

- Configurable register supporting DDR2 Registered DIMM applications
- Configurable to 25-bit 1 : 1 mode or 14-bit 1 : 2 mode
- Controlled output impedance drivers enable optimal signal integrity and speed
- Meets SSTUB32864 JEDEC specification speed performance
- Supports up to 450 MHz clock frequency of operation
- Optimized pinout for high-density DDR2 module design
- Chip-selects minimize power consumption by gating data outputs from changing state
- Supports SSTL_18 data inputs
- Differential clock (CK and $\overline{CK}$) inputs
- Supports LVCMOS switching levels on the control and $\overline{RESET}$ inputs
- Single 1.8 V supply operation (1.7 V to 2.0 V)
- Available in 96-ball, 13.5 mm × 5.5 mm, 0.8 mm ball pitch LFBGA package

3. Applications

- 400 MT/s to 800 MT/s DDR2 registered DIMMs without parity

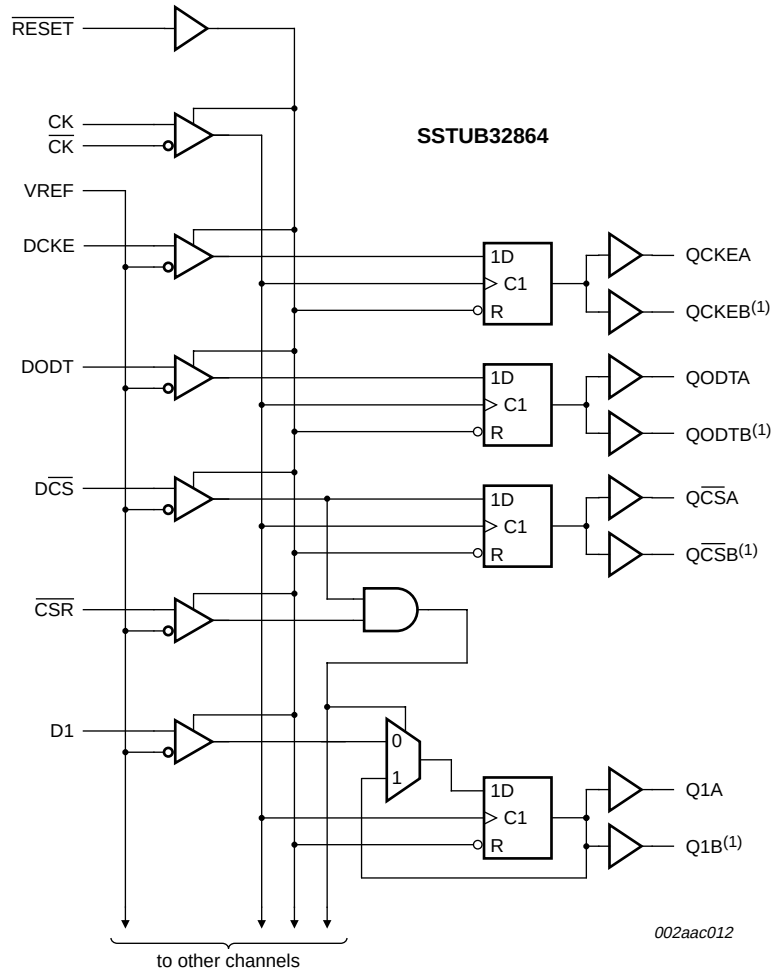
4. Ordering information

Table 1. Ordering information

T_{amb} = 0 °C to +70 °C.

Type number	Solder process	Package		
		Name	Description	Version
SSTUB32864EC/G	Pb-free (SnAgCu solder ball compound)	LFBGA96	plastic low profile fine-pitch ball grid array package; 96 balls; body 13.5 × 5.5 × 1.05 mm	SOT536-1

5. Functional diagram



(1) Disabled in 1 : 1 configuration.

Fig 1. Functional diagram of SSTUB32864; 1 : 2 mode (positive logic)

6. Pinning information

6.1 Pinning

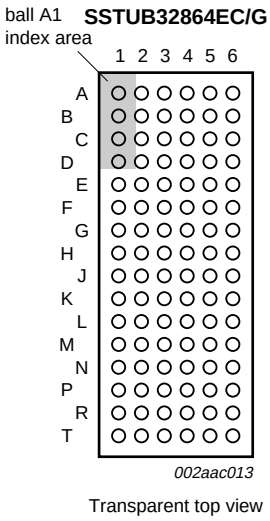


Fig 2. Pin configuration for LFBGA96

	1	2	3	4	5	6
A	DCKE	n.c.	VREF	V_{DD}	QCKE	DNU
B	D2	D15	GND	GND	Q2	Q15
C	D3	D16	V_{DD}	V_{DD}	Q3	Q16
D	DODT	n.c.	GND	GND	QODT	DNU
E	D5	D17	V_{DD}	V_{DD}	Q5	Q17
F	D6	D18	GND	GND	Q6	Q18
G	n.c.	$\overline{\text{RESET}}$	V_{DD}	V_{DD}	C1	C0
H	CK	$\overline{\text{DCS}}$	GND	GND	$\overline{\text{QCS}}$	DNU
J	$\overline{\text{CK}}$	$\overline{\text{CSR}}$	V_{DD}	V_{DD}	ZOH	ZOL
K	D8	D19	GND	GND	Q8	Q19
L	D9	D20	V_{DD}	V_{DD}	Q9	Q20
M	D10	D21	GND	GND	Q10	Q21
N	D11	D22	V_{DD}	V_{DD}	Q11	Q22
P	D12	D23	GND	GND	Q12	Q23
R	D13	D24	V_{DD}	V_{DD}	Q13	Q24
T	D14	D25	VREF	V_{DD}	Q14	Q25

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Fig 3. Ball mapping; 1 : 1 register (C0 = 0, C1 = 0); top view

	1	2	3	4	5	6
A	DCKE	n.c.	VREF	V_{DD}	QCKEA	QCKEB
B	D2	DNU	GND	GND	Q2A	Q2B
C	D3	DNU	V_{DD}	V_{DD}	Q3A	Q3B
D	DODT	n.c.	GND	GND	QODTA	QODTB
E	D5	DNU	V_{DD}	V_{DD}	Q5A	Q5B
F	D6	DNU	GND	GND	Q6A	Q6B
G	n.c.	$\overline{\text{RESET}}$	V_{DD}	V_{DD}	C1	C0
H	CK	$\overline{\text{DCS}}$	GND	GND	$\overline{\text{QCS}}$A	$\overline{\text{QCS}}$B
J	$\overline{\text{CK}}$	$\overline{\text{CSR}}$	V_{DD}	V_{DD}	ZOH	ZOL
K	D8	DNU	GND	GND	Q8A	Q8B
L	D9	DNU	V_{DD}	V_{DD}	Q9A	Q9B
M	D10	DNU	GND	GND	Q10A	Q10B
N	D11	DNU	V_{DD}	V_{DD}	Q11A	Q11B
P	D12	DNU	GND	GND	Q12A	Q12B
R	D13	DNU	V_{DD}	V_{DD}	Q13A	Q13B
T	D14	DNU	VREF	V_{DD}	Q14A	Q14B

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Fig 4. Ball mapping; 1 : 2 register A (C0 = 0, C1 = 1); top view

	1	2	3	4	5	6
A	D1	n.c.	VREF	V_{DD}	Q1A	Q1B
B	D2	DNU	GND	GND	Q2A	Q2B
C	D3	DNU	V_{DD}	V_{DD}	Q3A	Q3B
D	D4	n.c.	GND	GND	Q4A	Q4B
E	D5	DNU	V_{DD}	V_{DD}	Q5A	Q5B
F	D6	DNU	GND	GND	Q6A	Q6B
G	n.c.	$\overline{\text{RESET}}$	V_{DD}	V_{DD}	C1	C0
H	CK	$\overline{\text{DCS}}$	GND	GND	$\overline{\text{QCS}}$A	$\overline{\text{QCS}}$B
J	$\overline{\text{CK}}$	$\overline{\text{CSR}}$	V_{DD}	V_{DD}	ZOH	ZOL
K	D8	DNU	GND	GND	Q8A	Q8B
L	D9	DNU	V_{DD}	V_{DD}	Q9A	Q9B
M	D10	DNU	GND	GND	Q10A	Q10B
N	DODT	DNU	V_{DD}	V_{DD}	QODTA	QODTB
P	D12	DNU	GND	GND	Q12A	Q12B
R	D13	DNU	V_{DD}	V_{DD}	Q13A	Q13B
T	DCKE	DNU	VREF	V_{DD}	QCKEA	QCKEB

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Fig 5. Ball mapping; 1 : 2 register B (C0 = 1, C1 = 1); top view

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Type	Description
GND	B3, B4, D3, D4, F3, F4, H3, H4, K3, K4, M3, M4, P3, P4	ground input	ground
V_{DD}	A4, C3, C4, E3, E4, G3, G4, J3, J4, L3, L4, N3, N4, R3, R4, T4	1.8 V nominal	power supply voltage
VREF	A3, T3	0.9 V nominal	input reference voltage
ZOH	J5	input	reserved for future use
ZOL	J6	input	reserved for future use
CK	H1	differential input	positive master clock input
$\overline{CK}$	J1	differential input	negative master clock input
C0, C1	G6, G5	LVCMOS inputs	configuration control inputs
$\overline{RESET}$	G2	LVCMOS input	Asynchronous reset input (active LOW). Resets registers and disables VREF data and clock differential-input receivers.
$\overline{CSR}$, $\overline{DCS}$	J2, H2	SSTL_18 input	Chip select inputs (active LOW). Disables data outputs switching when both inputs are HIGH.[2]
D1 to D25	[1]	SSTL_18 input	Data inputs. Clocked in on the crossing of the rising edge of CK and the falling edge of $\overline{CK}$.
DODT	[1]	SSTL_18 input	The outputs of this register will not be suspended by $\overline{DCS}$ and $\overline{CSR}$ control.
DCKE	[1]	SSTL_18 input	The outputs of this register will not be suspended by $\overline{DCS}$ and $\overline{CSR}$ control.
Q1 to Q25, Q1A to Q14A, Q1B to Q14B	[1]	1.8 V CMOS	outputs that are suspended by $\overline{DCS}$ and $\overline{CSR}$ control[3]
Q$\overline{CS}$, Q$\overline{CS}$A, Q$\overline{CS}$B	[1]	1.8 V CMOS	data outputs that will not be suspended by $\overline{DCS}$ and $\overline{CSR}$ control
QODT, QODTA, QODTB	[1]	1.8 V CMOS	data outputs that will not be suspended by $\overline{DCS}$ and $\overline{CSR}$ control
QCKE, QCKEA, QCKEB	[1]	1.8 V CMOS	data outputs that will not be suspended by $\overline{DCS}$ and $\overline{CSR}$ control
n.c.	A2, D2, G1	-	Not connected. Ball present but no internal connection to the die.
DNU	[1]	-	Do-not-use. Ball internally connected to the die which should be left open-circuit.

[1] Depends on configuration. See Figure 3, Figure 4, and Figure 5 for ball number.

[2] Configurations:
Data inputs = D2, D3, D5, D6, D8 to D25 when C0 = 0 and C1 = 0.
Data inputs = D2, D3, D5, D6, D8 to D14 when C0 = 0 and C1 = 1.
Data inputs = D1 to D6, D8 to D10, D12, D13 when C0 = 1 and C1 = 1.

[3] Configurations:
Data outputs = Q2, Q3, Q5, Q6, Q8 to Q25 when C0 = 0 and C1 = 0.
Data outputs = Q2, Q3, Q5, Q6, Q8 to Q14 when C0 = 0 and C1 = 1.
Data outputs = Q1 to Q6, Q8 to Q10, Q12, Q13 when C0 = 1 and C1 = 1.

7. Functional description

7.1 Function table

Table 3. Function table (each flip-flop)

L = LOW voltage level; H = HIGH voltage level; X = don't care; ↑ = LOW-to-HIGH transition; ↓ = HIGH-to-LOW transition

Inputs						Outputs[1]		
$\overline{RESET}$	$D\overline{CS}$	$\overline{CSR}$	CK	$\overline{CK}$	Dn, DODT, DCKE	Qn	$Q\overline{CS}$	QODT, QCKE
H	L	L	↑	↓	L	L	L	L
H	L	L	↑	↓	H	H	L	H
H	L	L	L or H	L or H	X	Q_0	Q_0	Q_0
H	L	H	↑	↓	L	L	L	L
H	L	H	↑	↓	H	H	L	H
H	L	H	L or H	L or H	X	Q_0	Q_0	Q_0
H	H	L	↑	↓	L	L	H	L
H	H	L	↑	↓	H	H	H	H
H	H	L	L or H	L or H	X	Q_0	Q_0	Q_0
H	H	H	↑	↓	L	Q_0	H	L
H	H	H	↑	↓	H	Q_0	H	H
H	H	H	L or H	L or H	X	Q_0	Q_0	Q_0
L	X or floating	X or floating	X or floating	X or floating	X or floating	L	L	L

[1] Q_0 is the previous state of the associated output.

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		–0.5	+2.5	V
V_I	input voltage	receiver	–0.5[1]	+2.5[2]	V
V_O	output voltage	driver	–0.5[1]	V_{DD} + 0.5[2]	V
I_{IK}	input clamping current	$V_I < 0$ V or $V_I > V_{DD}$	-	±50	mA
I_{OK}	output clamping current	$V_O < 0$ V or $V_O > V_{DD}$	-	±50	mA
I_O	output current	continuous; $0 V < V_O < V_{DD}$	-	±50	mA
I_{CCC}	continuous current through each V_{DD} or GND pin		-	±100	mA
T_{stg}	storage temperature		–65	+150	°C

[1] The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

[2] This value is limited to 2.5 V maximum.

9. Recommended operating conditions

Table 5. Operating conditions

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DD}	supply voltage			1.7	-	2.0	V
V_{ref}	reference voltage			$0.49 \times V_{DD}$	$0.50 \times V_{DD}$	$0.51 \times V_{DD}$	V
V_T	termination voltage			V_{ref} – 0.040	V_{ref}	V_{ref} + 0.040	V
V_I	input voltage			0	-	V_{DD}	V
$V_{IH(AC)}$	AC HIGH-level input voltage	data inputs (Dn), $\overline{CSR}$		V_{ref} + 0.250	-	-	V
$V_{IL(AC)}$	AC LOW-level input voltage	data inputs (Dn), $\overline{CSR}$		-	-	V_{ref} – 0.250	V
$V_{IH(DC)}$	DC HIGH-level input voltage	data inputs (Dn), $\overline{CSR}$		V_{ref} + 0.125	-	-	V
$V_{IL(DC)}$	DC LOW-level input voltage	data inputs (Dn), $\overline{CSR}$		-	-	V_{ref} – 0.125	V
V_{IH}	HIGH-level input voltage	$\overline{RESET}$, Cn	[1]	$0.65 \times V_{DD}$	-	V_{DD}	V
V_{IL}	LOW-level input voltage	$\overline{RESET}$, Cn	[1]	-	-	$0.35 \times V_{DD}$	V
V_{ICR}	common mode input voltage range	CK, $\overline{CK}$	[2]	0.675	-	1.125	V
V_{ID}	differential input voltage	CK, $\overline{CK}$	[2]	600	-	-	mV
I_{OH}	HIGH-level output current			-	-	–8	mA
I_{OL}	LOW-level output current			-	-	8	mA
T_{amb}	ambient temperature	operating in free air		0	-	+70	°C

[1] The $\overline{RESET}$ and Cn inputs of the device must be held at valid logic levels (not floating) to ensure proper device operation.

[2] The differential inputs must not be floating, unless $\overline{RESET}$ is LOW.

10. Characteristics

Table 6. Characteristics

Recommended operating conditions; T_{amb} = 0 °C to +70 °C; all voltages are referenced to GND (ground = 0 V); unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	HIGH-level output voltage	I_{OH} = –6 mA; V_{DD} = 1.7 V	1.2	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 6 mA; V_{DD} = 1.7 V	-	-	0.5	V
I_I	input current	all inputs; $V_I = V_{DD}$ or GND; V_{DD} = 2.0 V	–5	-	+5	µA
I_{DD}	supply current	static Standby mode; $\overline{RESET}$ = GND; I_O = 0 mA; V_{DD} = 2.0 V	-	-	2	mA
		static Operating mode; $\overline{RESET} = V_{DD}$; I_O = 0 mA; V_{DD} = 2.0 V; $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$	-	-	40	mA
I_{DDD}	dynamic operating current per MHz	clock only; $\overline{RESET} = V_{DD}$; $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$; CK and $\overline{CK}$ switching at 50 % duty cycle. I_O = 0 mA; V_{DD} = 2.0 V	-	16	-	µA
		per each data input, 1 : 1 mode; $\overline{RESET} = V_{DD}$; $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$; CK and $\overline{CK}$ switching at 50 % duty cycle. One data input switching at half clock frequency, 50 % duty cycle. I_O = 0 mA; V_{DD} = 2.0 V	-	11	-	µA
		per each data input, 1 : 2 mode; $\overline{RESET} = V_{DD}$; $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$; CK and $\overline{CK}$ switching at 50 % duty cycle. One data input switching at half clock frequency, 50 % duty cycle. I_O = 0 mA; V_{DD} = 2.0 V	-	19	-	µA
C_i	input capacitance	data inputs, $\overline{CSR}$; $V_I = V_{ref} \pm 250$ mV; V_{DD} = 1.8 V	2.5	-	3.5	pF
		CK and $\overline{CK}$; V_{ICR} = 0.9 V; V_{ID} = 600 mV; V_{DD} = 1.8 V	2	-	3	pF
		$\overline{RESET}$; $V_I = V_{DD}$ or GND; V_{DD} = 1.8 V	2	-	4	pF

Table 7. Timing requirements

Recommended operating conditions; T_{amb} = 0 °C to +70 °C; V_{DD} = 1.8 V ± 0.1 V; unless otherwise specified. See Figure 6 through Figure 11.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{clock}	clock frequency			-	-	450	MHz
t_W	pulse width	CK, $\overline{CK}$ HIGH or LOW		1	-	-	ns
t_{ACT}	differential inputs active time		[1][2]	-	-	10	ns
t_{INACT}	differential inputs inactive time		[1][3]	-	-	15	ns
t_{su}	set-up time	$\overline{DCS}$ before CK ↑, $\overline{CK}$ ↓, $\overline{CSR}$ HIGH		0.6	-	-	ns
		$\overline{DCS}$ before CK ↑, $\overline{CK}$ ↓, $\overline{CSR}$ LOW		0.5	-	-	ns
		$\overline{CSR}$, ODT, CKE, and data before CK ↑, $\overline{CK}$ ↓		0.5	-	-	ns
t_h	hold time	$\overline{DCS}$, $\overline{CSR}$, ODT, CKE, and data after CK ↑, $\overline{CK}$ ↓		0.4	-	-	ns

[1] This parameter is not necessarily production tested.

[2] Data inputs must be active below a minimum time of $t_{ACT(max)}$ after $\overline{RESET}$ is taken HIGH.

[3] Data and clock inputs must be held at valid levels (not floating) a minimum time of $t_{INACT(max)}$ after $\overline{RESET}$ is taken LOW.

Table 8. Switching characteristics

Recommended operating conditions; T_{amb} = 0 °C to +70 °C; V_{DD} = 1.8 V ± 0.1 V; Class I, $V_{ref} = V_T = V_{DD} \times 0.5$ and C_L = 10 pF; unless otherwise specified. See Figure 6 through Figure 11.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{max}	maximum input clock frequency			450	-	-	MHz
t_{PDM}	peak propagation delay	CK and $\overline{CK}$ to output	[1]	1.1	-	1.5	ns
t_{PDMSS}	simultaneous switching peak propagation delay	CK and $\overline{CK}$ to output	[1][2]	-	-	1.6	ns
t_{PHL}	HIGH-to-LOW propagation delay	$\overline{RESET}$ to output		-	-	3	ns

[1] Includes 350 ps of test-load transmission line delay.

[2] This parameter is not necessarily production tested.

Table 9. Output edge rates

Recommended operating conditions; V_{DD} = 1.8 V ± 0.1 V; unless otherwise specified.

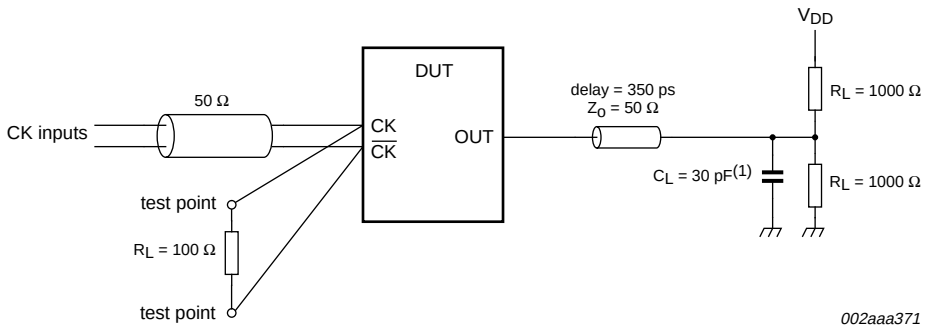
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
dV/dt_r	rising edge slew rate		1	-	4	V/ns
dV/dt_f	falling edge slew rate		1	-	4	V/ns
dV/dt_Δ	absolute difference between dV/dt_r and dV/dt_f		-	-	1	V/ns

11. Test information

11.1 Test circuit

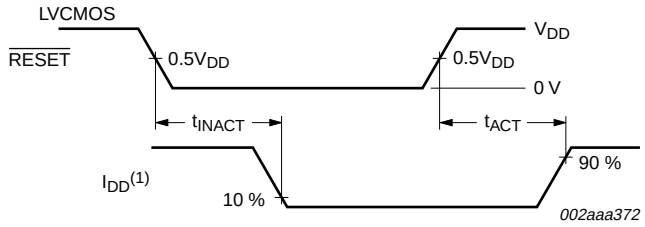
All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz; Z_O = 50 Ω; input slew rate = 1 V/ns ± 20 %, unless otherwise specified.

The outputs are measured one at a time with one transition per measurement.



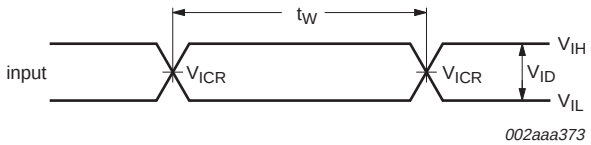
(1) C_L includes probe and jig capacitance.

Fig 6. Load circuit



(1) I_{DD} tested with clock and data inputs held at V_{DD} or GND, and I_O = 0 mA.

Fig 7. Voltage and current waveforms; inputs active and inactive times

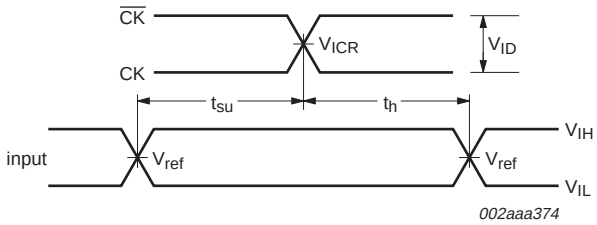


V_{ID} = 600 mV.

$V_{IH} = V_{ref}$ + 250 mV (AC voltage levels) for differential inputs. $V_{IH} = V_{DD}$ for LVCMOS inputs.

$V_{IL} = V_{ref}$ – 250 mV (AC voltage levels) for differential inputs. V_{IL} = GND for LVCMOS inputs.

Fig 8. Voltage waveforms; pulse duration



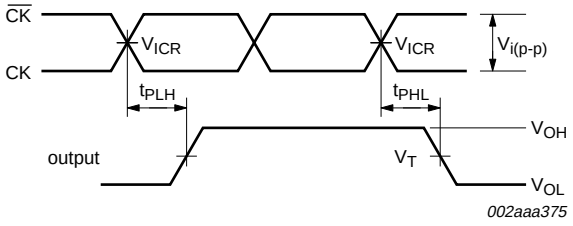
V_{ID} = 600 mV.

$V_{ref} = 0.5V_{DD}$.

$V_{IH} = V_{ref}$ + 250 mV (AC voltage levels) for differential inputs. $V_{IH} = V_{DD}$ for LVCMOS inputs.

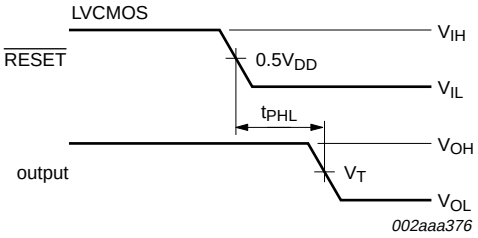
$V_{IL} = V_{ref}$ – 250 mV (AC voltage levels) for differential inputs. V_{IL} = GND for LVCMOS inputs.

Fig 9. Voltage waveforms; set-up and hold times



t_{PLH} and t_{PHL} are the same as t_{PD}.

Fig 10. Voltage waveforms; propagation delay times (clock to output)



t_{PLH} and t_{PHL} are the same as t_{PD}.

$V_{IH} = V_{ref}$ + 250 mV (AC voltage levels) for differential inputs. $V_{IH} = V_{DD}$ for LVCMOS inputs.

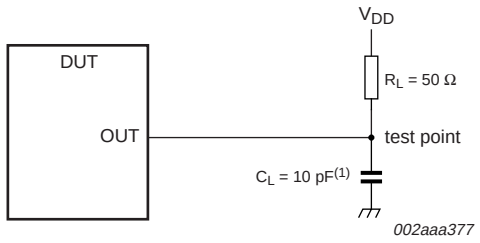
$V_{IL} = V_{ref}$ – 250 mV (AC voltage levels) for differential inputs. V_{IL} = GND for LVCMOS inputs.

Fig 11. Voltage waveforms; propagation delay times (reset to output)

11.2 Output slew rate measurement

V_{DD} = 1.8 V ± 0.1 V.

All input pulses are supplied by generators having the following characteristics:
PRR ≤ 10 MHz; Z_0 = 50 Ω; input slew rate = 1 V / ns ± 20 %, unless otherwise specified.



(1) C_L includes probe and jig capacitance.

Fig 12. Load circuit, HIGH-to-LOW slew measurement

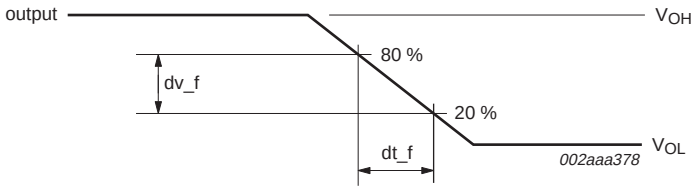
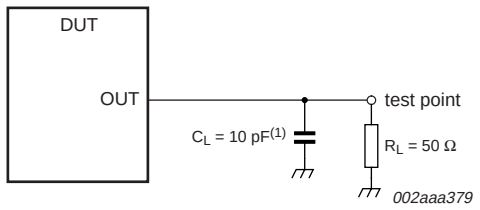


Fig 13. Voltage waveforms, HIGH-to-LOW slew rate measurement



(1) C_L includes probe and jig capacitance.

Fig 14. Load circuit, LOW-to-HIGH slew measurement

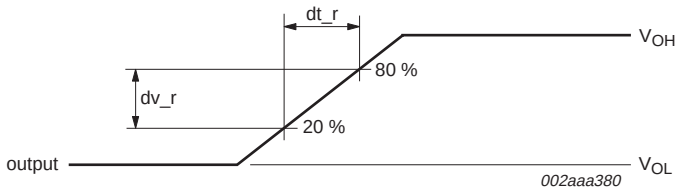
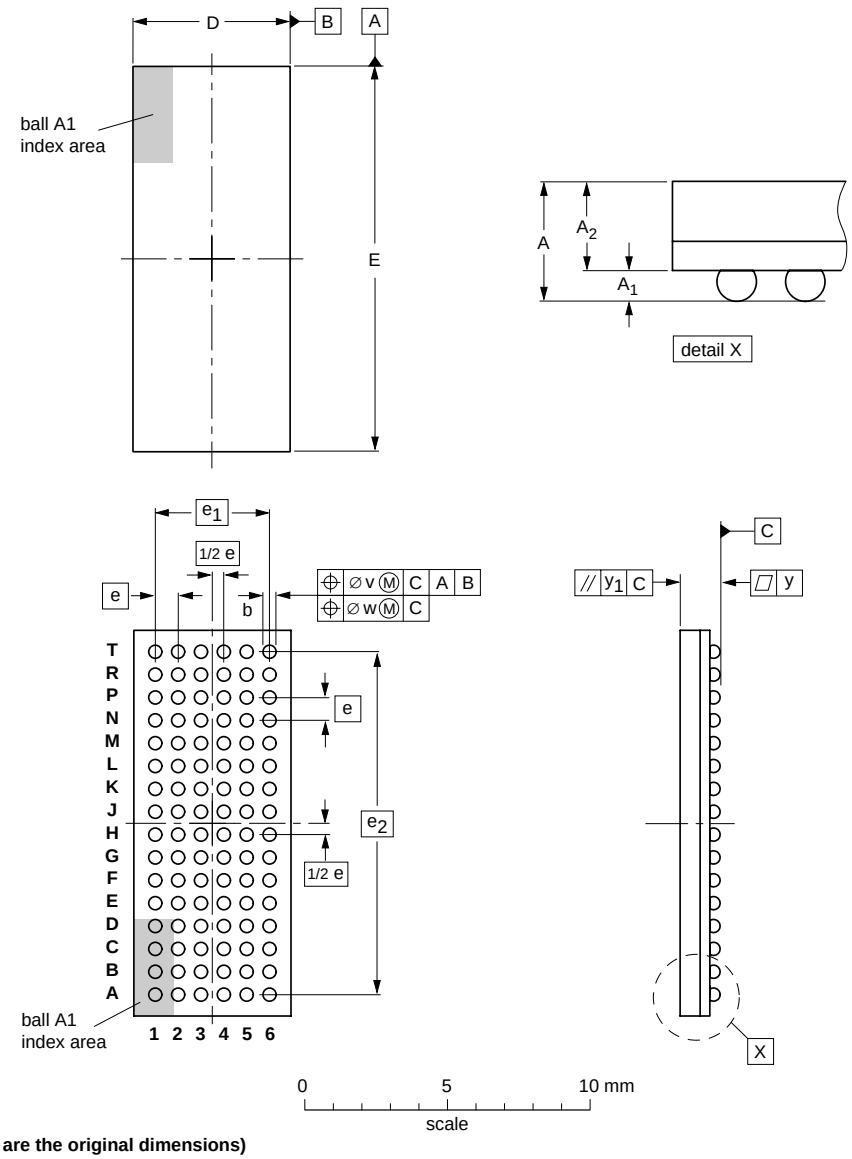


Fig 15. Voltage waveforms, LOW-to-HIGH slew rate measurement

12. Package outline

LFBGA96: plastic low profile fine-pitch ball grid array package; 96 balls; body 13.5 x 5.5 x 1.05 mm SOT536-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	1.5	0.41 0.31	1.2 0.9	0.51 0.41	5.6 5.4	13.6 13.4	0.8	4	12	0.15	0.1	0.1	0.2

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT536-1						~~00-03-04~~ 03-02-05

Fig 16. Package outline SOT536-1 (LFBGA96)

13. Soldering

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

13.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

13.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus PbSn soldering

13.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

13.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 17) than a PbSn process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 10 and 11

Table 10. SnPb eutectic process (from J-STD-020C)

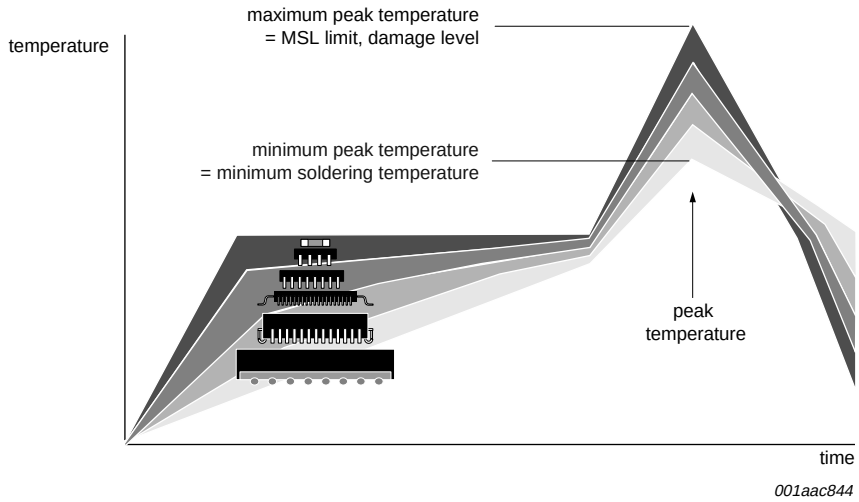
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 11. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 17.



MSL: Moisture Sensitivity Level

Fig 17. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

14. Abbreviations

Table 12. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DDR	Double Data Rate
DIMM	Dual In-line Memory Module
LVCMOS	Low Voltage Complementary Metal Oxide Semiconductor
PRR	Pulse Repetition Rate
RDIMM	Registered Dual In-line Memory Module
SSTL	Stub Series Terminated Logic

15. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
SSTUB32864_2	20070326	Product data sheet	-	SSTUB32864_1
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Table 6 "Characteristics", symbol I_{DD} (max.) changed from "100 µA" to "2 mA".			
SSTUB32864_1	20060421	Product data sheet	-	-

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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